Additive-Driven Assembly of Block Copolymer–Nanoparticle Hybrid Materials for Solution Processable Floating Gate Memory

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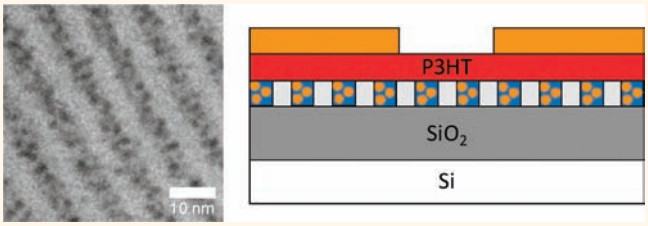
ABSTRACT



Floating gate memory devices were fabricated using well-ordered gold nanoparticle/block copolymer hybrid films as the charge trapping layers, SiO_2 as the dielectric layer, and poly-(3-hexylthiophene) as the semiconductor layer. The charge trapping layer was prepared *via* self-assembly. The addition of Au nanoparticles that selectively hydrogen bond with pyridine in a poly(styrene-*b*-2-vinyl pyridine) block copolymer yields well-ordered hybrid materials at Au nanoparticle loadings up to 40 wt %. The characteristics of the memory window were tuned by simple control of the Au nanoparticle concentration. This approach enables the fabrication of well-ordered charge storage layers by solution processing, which is extendable for the fabrications of large area and high density devices *via* roll-to-roll processing.

KEYWORDS: block copolymer · nanoparticle · hybrid material · floating gate memory · transistor

Organic memory is an emerging technology with potential to realize low cost, large area, and flexible charge storage media.[1−5] Among different types of memory devices, floating gate organic field effect transistor (OFET) memory devices are the most widely used form because of their simple structure, nondestructive read-out, and complementary integrated circuit architechtural compatibility.[1,5] The difference between OFET memory devices and a simple OFET is that the former contains charge trapping layers comprising metal or semiconductor domains immersed in a dielectric layer. The charge can be stored or erased in this layer by applying gate voltage. To achieve such device structure, it is common to deposit a thin layer of metal between two dielectric layers (a thin tunneling layer and a thick blocking layer).[3,6,7] However, the successive deposition of these layers in high vacuum is not desirable for fast, low-cost roll-to-roll printing processes, which is a significant potential advantage of organic electronic devices. An alternative approach is to employ metal nanoparticles (NPs) dispersed in a polymer dielectric as the charge trapping element.[8,9] This layer could then be coated onto the device using solution processing.

The incorporation of NPs within well-ordered block copolymer templates (BCPs) could be an ideal approach to the charge trapping layer. Order in the composites and distribution of the NPs can be controlled by the polymer template; BCPs spontaneously form ordered periodic nanoscale spherical, cylindrical, or lamellar morphologies of controlled domain spacing when cast from solution.[10−12] Recently, Leong *et al.* reported the *in situ* synthesis of gold NPs in poly(styrene-*b*-4-vinyl pyridine) and its application in organic floating gate memory devices.[13,14] It was demonstrated that block copolymer could function as a tunneling layer in transistor memory devices. However, the *in situ* synthesis of NPs in block copolymer is generally done at very low concentrations of NPs to minimize particle aggregation. The low concentration of NPs in the block copolymer results in a small memory window for the devices.

The successful use of BCPs as templates for nanoparticle/polymer hybrids generally will require control over both the distribution and loading of the NPs within the target domains. One especially difficult challenge

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has been the preparation of well-ordered hybrid NP/BCP systems that contain sufficient concentrations of NPs required for many practical device applications. Once achieved, these strategies could be employed for the solution phase fabrication of devices on flexible and roll-to-roll process platforms.

The behavior of NP BCP systems has been extensively studied using both experiment and theory. Early work by Kramer, Russell, and others demonstrated good control of the distribution of low concentrations of NPs in block copolymer hosts using ligands or mixed ligand systems that were chemically similar to the block copolymer segments or that exhibited weak interactions with the chain segments.[15−23] It is well understood that the addition of NPs to block copolymers carries a significant entopic penalty associated with the stretching of the BCP chain segments required to accommodate the NPs.[24,25] For systems with weak interactions, these penalties can push the hybrid system toward disorder and can dominate behavior, resulting in a strict upper bound on NP loading. To achieve the high NP loadings necessary for many device applications, the entropic constraints must be mitigated or overcome by enthapically favorable interactions between the NP and BCP. Zhao *et al*. reported the assembly of ordered polymer/NP assemblies in which the particles reside within domains consisting of short organic side chains associated with one of the BCP segments in the hierarchical assembly *via* hydrogen bonding.[26] While the interaction between the particles and side chains is weak, the prevalence of chain ends may reduce the stretching penalty. On the other hand, Warren *et al*. prepared mesoporous metals in which metal NPs coated with an organic shell consisting of ionic liquid coatings were coassembled with specially designed BCPs.[27] While this study employed specific chemistries and tedious preparation protocols, it indicated that favorable interactions between a NP and BCP can yield ordered materials at high NP concentrations. Studies of well ordered hybrid systems are nontheless still quite limited, and the preparation of materials containing high concentrations of NPs remains challenging. Consequently few applications for functional electronic devices have been explored.

In this study we present a simple approach for the preparation of well-ordered polymer/NP composites through the concept of additive-driven assembly,[28] and its application for organic floating gate memory devices. Recently, we developed a general pathway for achieving well-ordered hybrid materials using nanoparticles functionalized with short organic ligands or organic additives that can hydrogen bond to one segment of a BCP template.[29−31] This strong, selective, ethalpic interaction drives the assembly of block copolymers and overcomes entropic barriers to high NP loadings . For example, gold NPs that selectively hydrogen bond with one of the segments of a

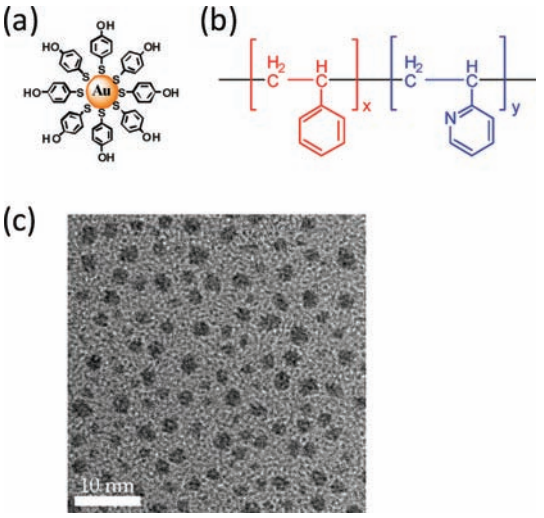

Figure 1. (a) Schematic representation of Au NPs with multiple H-bond-donating groups, (b) chemical structure of PS-P2VP, and (c) TEM image of synthesized Au NPs.

poly-(ethylene oxide-*b*-propylene oxide-*b*-ethylene oxide) (PEO-PPO-PEO) or poly(styrene-*b*-ethylene oxide) (PS-PEO) block copolymer is shown to induce order in otherwise disordered systems.[28] The loadings of the NPs can achieve more than 40%, while the ordered structure can be maintained. We consider this to be a nearly ideal system for floating gate memory device applications since it enables facile control of the density of Au NPs, and we can prepare the charge trapping layers and tunneling layers by the spin coating of the block copolymer and Au NPs mixture in a single step. This process is also compatible with roll-to-roll print techniques which are a significant advantage for organic electronic devices compared with their inorganic counterparts.

RESULTS AND DISCUSSION

Figure 1 shows the materials used in this study. 4-Hydroxythiophenol-functionalized Au (Au−OH) NPs were prepared using literature procedures.[32] Thermogravimetric analysis (TGA) indicated that the Au content of the Au−OH NPs was ~72.3 wt %. Poly(styrene-*b*-2-vinyl pyridine) (PS-P2VP, M_n = 16.5 kDa, PDI = 1.09, P2VP weight fraction (f_{P2VP}) = 0.50; denoted as PS8.2k-*b*-P2VP8.3k) was used as a template. (The 2-vinyl pyridine segments serves as the hydrogen bond acceptor, whereas the hydroxythiophenol ligands are the donor.) The synthesized Au−OH NPs are very uniform with an average size of *ca*. 2.0 nm as indicated by transmission electron microscopy (TEM) (Figure 1c). Figure 2a shows small-angle X-ray scattering (SAXS) profiles for PS-P2VP and blends of this BCP with Au−OH NPs at several NP concentrations. We express the concentrations of the NPs as a wt % of the composite based on the mass of the NP core and ligand shell. Neat PS-P2VP shows one peak suggesting there is microphase separation in the block copolymer. The addition of 10 wt % Au−OH NPs increased the

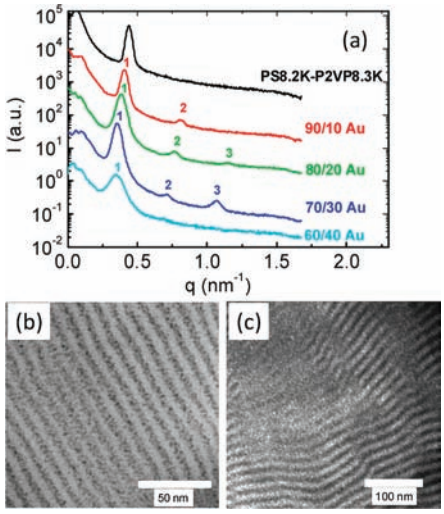

Figure 2. (a) SAXS profiles of PS-P2VP with Au NPs at 0, 10, 20, 30, and 40 wt % concentration; TEM images of a blend of PS-P2VP with (b) 20 wt % Au NPs and (c) 40 wt % Au NPs.

segregation strength and order within the composite film, and higher order peaks are observed in the SAXS profile. For the 20 wt % and 30 wt % Au−OH NPs, the scattering data showed a third-order peak at a *q* value three times that of the first, suggesting a lamellar morphology. TEM (Figure 2b) confirmed this structure. When the NP concentration was increased to 40 wt %, the film was still strongly segregated, but the scattering profiles suggest the onset of a transition between ordered morphologies (Figure 2c). Lower magnification TEM images are shown in the Supporting Information, Figure S1. This observation is consistent with previous studies in the poly(styrene-*b*-ethylene oxide) (PS-b-PEO)/Au−OH NPs system.[28] It is further suggested that this approach is applicable to a wide range of nanoparticles and block copolymers, and is a general approach to prepare well-ordered hybrid materials.

The interaction between the Au−OH NPs and P2VP is in fact very strong. When the tetrahydrofuran (THF) solution of Au−OH NPs was dropped in THF solution of P2VP homopolymer, precipitation was observed. This suggests that the Au−OH NPs physically cross-link P2VP *via* H-bonding resulting in precipitation of the complex from the THF solvent. By contrast, a mixture of THF solution of Au−OH NPs and a THF solution of PS-P2VP still yields a stable optically clear solution (Supporting Information, Figure S2). Here we point out that while charge trapping layers could in principle comprise well-distributed Au NPs in the P2VP homopolymer, the aggregation and precipitation of the Au-NP/homo-P2VP complex from solution rendered solution preparation of the active layer from these components impractical. The mixture of Au NPs and the random copolymer of PS-P2VP could also be used as charge trapping layers; however, a random copolymer containing 50% PVP did not prevent aggregation of the Au NPs in the solution. Thus the BCP offers practical processing advantages.

The operation of floating gate OFET memory devices relies on charge trapping in layers comprising metals or semiconductors immersed in a dielectric. The charge carriers can be programmed or erased in this layer by applying gate voltage. Here, we can prepare such charge trapping layers by a simple spin coating of the blended solution of Au−OH NPs and PS-P2VP. Figure 3a shows the structure of the devices used in this study. Transistors with a channel length (*L*) of 100 μm and width (*W*) of 3 mm were fabricated in a bottom-gate configuration using highly doped Si as the gate electrode. A PS-P2VP layer with or without Au NPs was spin coated on a SiO_2 layer used as the gate dielectric. The thickness of the PS-P2VP was approximately 30 nm as measured by surface profilometry. A *ca.* 10 nm thick P3HT film was transferred by contact film transfer (CFT) method on the top of PS-P2VP layer. The preparation of FETs by the CFT method has been described previously.[33,34] Water-soluble polymers sodium poly(styrenesulfonate) (PSS) act as a "sacrificial layer" in the transfer process. Briefly, a film with a structure of glass/PSS/P3HT was prepared by successive spin coating of an aqueous solution of PSS and a chlorobenzene solution of P3HT (2 mg/mL). This polymer film was gently brought into contact with the surface of the PS-P2VP/SiO_2 layer with the polymer face down. One drop of water was placed on the edge of the stacked substrates. After the water flowed from one side of the substrate to the other, the glass substrate was detached from the organic layer, resulting in the transfer of the polymer film from the glass to the surface of the PS-P2VP/SiO_2 layer. Gold electrodes were then evaporated onto the surface through a metal mask. The thickness of the P3HT layer was determined by X-ray reflectivity (XRR) measurements.

Figure 3b and Figure 3c show the electrical properties of the fabricated organic FETs without Au NPs to determine the charge trapping effects. The only difference compared with the memory devices was the absence of the Au NPs in the BCPs. Otherwise, all of the device structures and the processing conditions were identical. Figure 3b shows the typical output characteristics of the device. A clear field-effect and well-resolved linear and saturation regions are observed from the output curves. Figure 3c shows the transfer characteristics for both forward and reverse voltage scans from 20 to −100 V at V_{DS} = −10 V and V_{DS} = −80 V. The device exhibited almost no hysteresis in the transfer curves suggesting negligible charge trapping sites in the bulk and at the interface of the gate dielectric layer (PS-P2VP/SiO_2). The mobility values calculated from the saturation region and the linear region were μ_{sat} = 0.11 cm^2/(V s) and μ_{lin} = 0.06 cm^2/(V s), respectively. The transistor exhibited a threshold voltage of −17 V and an on/off ratio greater than 10^6.

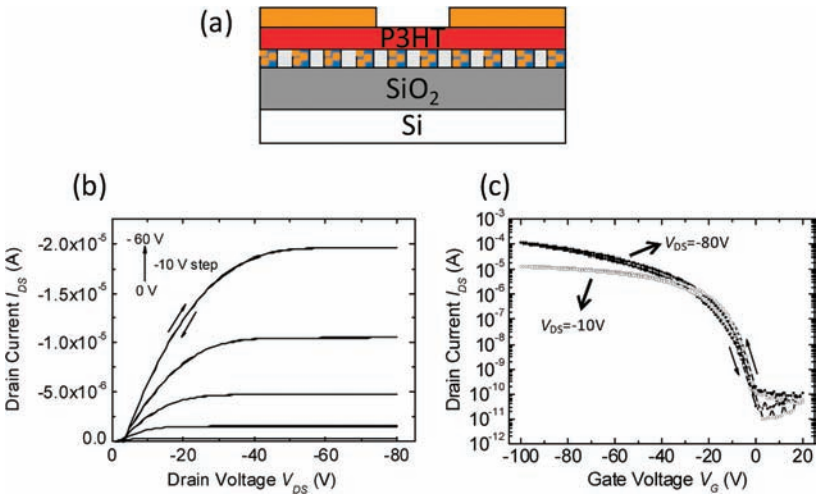

Figure 3. (a) Schematic representation of the memory devices used in this study; (b) output curves and (c) transfer curves of the device without Au NPs.

The mobility value of the P3HT transistors here is comparable with the best devices reported in the literature.[35,36] Our devices also show very good reproducibility. More than 20 independent samples on PS-P2VP/SiO_2 were prepared by using the same process, and over 90% of them exhibited a linear mobility in the range of 0.05−0.10 $cm^2/(V\ s)$ and a saturated mobility in the range of 0.10−0.20 $cm^2/(V\ s)$.

To study the effect of the Au NPs in the dielectric layer, we varied the loading the Au NPs from 10% to 60%. Figure 4a shows the transfer characteristics of the device with 20% Au NP loading upon double sweeping from 20 to −100 V at V_{DS} = −10 V. The anticlockwise I_D-V_G hysteresis loop with a threshold voltage shift of 11 V indicates that there is a hole trapping effect, which is in contrast to the control devices as shown in Figure 3c. During the forward sweep, the carrier density in the semiconductor increases with the gate voltage, and the "lucky carrier" is injected from the P3HT to Au NPs. After Au NPs accept the charges, the electrical potential between the gate and source is changed, resulting in a shift of threshold voltage. The number of stored charges (Δn) can be determined from the shift in V_T according to $\Delta n = \Delta V_T \times C_i/e = 7.5 \times 10^{11}\ cm^{-2}$, where C_i is the capacitance of the dielectric layer and e is the elementary charge. Upon increasing the loading of Au NPs, larger hysteresis windows of the transfer curves upon double sweeping were clearly observed. As shown in Figure 4b, the shift of V_T is increased to 41 V when the loading of Au NPs was 40%. The density of stored carriers is calculated to be *ca.* $2.8 \times 10^{12}\ cm^{-2}$. When the loading of Au NPs increased to 60%, the hysteresis is still clearly observed. However, the off current (I_{off}) of the device is significantly increased from 10^{-11} to 10^{-7} A (Figure 4c), which could be attributed to charge percolation through aggregates of the Au NPs bridged in between source and drain (see Supporting Information, Figure S3). These results are consistent with SAXS observations. When the loading of the Au−OH NPs was less than 40%, all the NP/BCP composite was well ordered. Further addition of NPs up to 60 wt % led to a loss of the multiple higher-order reflections, suggesting an upper bound on the particle loading at which strong order can be maintained in this system. Figure 4d shows the plot threshold voltage shift during transfer characterization and I_{off} of the devices against the percentage of Au NPs loading. (The transfer curves of the devices with different amounts of Au NPs are shown in the Supporting Information, Figure S4.) The standard deviations are calculated from the analysis of 4−10 devices. The threshold voltage values are extracted from linear plots of V_G *versus* I_{DS}. For the devices with 60% Au NPs, the error bar is much larger than other points due to the difficulties in accurately extracting threshold voltages due to high off-current. The threshold voltage difference increases with the loading of the Au NPs with a superlinear relationship. This observation is interesting. It is known that the charge trapping mechanism in the floating gate memory is related to tunneling, and therefore the probability of charge trapping depends on distance from the interface of the trapping layer. At low Au NPs concentrations, it is expected that the distribution of NPs will be biased toward the center of the PVP domains to reduce the chain stretching contribution to free energy,[18] and therefore the distance between P3HT and Au NPs is not optimized. With increasing NP loading, the density of the Au NPs near the P3HT/PS-P2VP interface will increase, and the Au NPs near the P3HT layer should have a much higher probability to trap the charge. This observation suggests that high loading of Au NPs is significantly important to achieve a clear memory effect in floating gate memory. For the device with 40 wt % Au NP loading, the interparticle distance can be estimated to be approximately 4 nm by assuming the density of

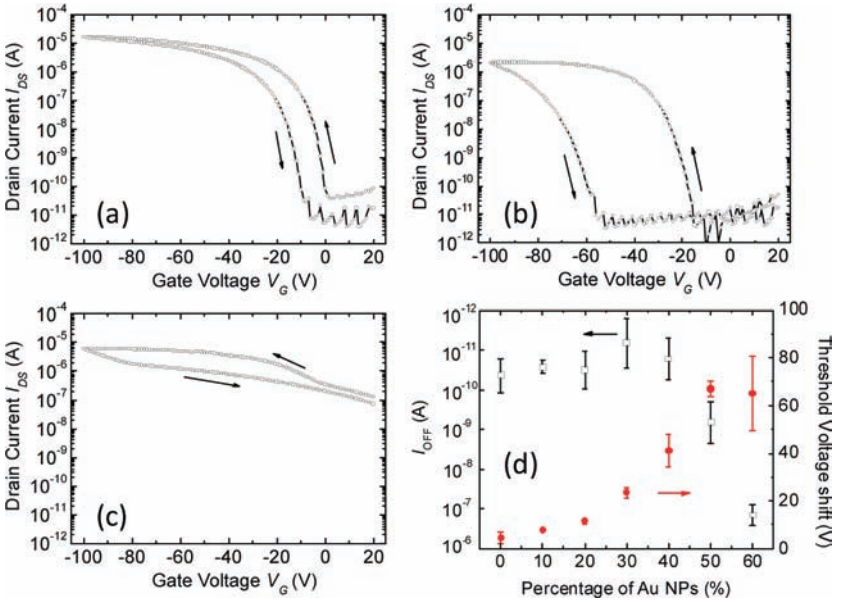

Figure 4. Double sweeping semilog plots of I_D-V_G transfer characteristics of the devices with (a) 20, (b) 40, and (c) 60 wt % Au NPs. The drain voltage (V_D) is −10 V. (d) Plots of threshold voltage shift and off current (I_{off}) of the memory devices with amount of Au NPs.

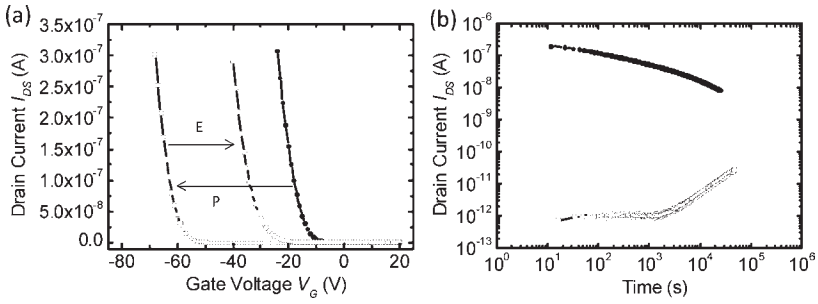

Figure 5. (a) Transfer curves of the organic memory devices according to the programming/erasing operations. Programming bias pulses of −100 V were applied to the gate for 1 s under dark, and erasing bias pulses of +100 V were applied to the gate for 1 s under illumination. (b) Data retention capability as a function of the retention time for the memory devices in the programmed/erased states.

Au NPs is 19.3 g/cm^3, the density of PS-P2VP is 1.0 g/cm^3, the diameter of the particles is 2.0 nm, and the PS/P2VP volume ratio is 1:1. For a 30 nm thick hybrid film, the areal density of Au NPs in the P2VP domain is approximately 3.57×10^{13} cm^{-2} while the areal density in the entire film (including the PS domains) is 1.79×10^{13} cm^{-2}, which is 2 orders of magnitude higher than the *in situ* synthesized Au NPs in BCPs in previous approaches to floating gate memory.[13] The calculation details are shown in the Supporting Information.

We further studied the performance of the devices as electrically programmable and erasable memory cells. In general, the programming and erasing procedures of such devices consist of the application of voltage pulses of fixed duration. Depending on the polarity of the voltage pulses, carriers can be injected into the floating gate. After pulsing occurred, the threshold voltage was determined by monitoring the transfer curves. We take the devices with 40% Au NPs loading. As shown in Figure 5a, the transfer curve of the transistor shifted toward negative voltages with a V_T shift of −43 V upon application of a programming voltage at −100 V for 1 s. The negative gate voltage pulses cause negative shifts in V_T indicating holes are injected from the P3HT channel into the Au NPs. However, the erasing operation seems more difficult by only changing the gate voltage under dark conditions. This observation is also reported in other systems probably due to the environment of Au NPs.[14] The erasing operation can be easily done under light illumination. After applying the gate voltage at 100 V for 1 s under illumination, the transfer curve shifted toward the positive voltage. This suggested that the charge trapped by the Au NPs were released during the erasing operations. Data retention experiments on an individual device suggested that the retention time can last over 10 hours while reading the device once every 10 s by applying a $V_G = -40$ V and a $V_{DS} = -10$ V for 1 s (more than 4000 device read-out operations)

(Figure 5b). We confirmed the device stability by reading the device every 500 s for more than 100 h, after which the transistor still had a read-current ratio higher than 10^2 (Supporting Information, Figure S5). Since charge loss occurs only during the read-out process, data retention without interrogation is expected to be much longer.

CONCLUSIONS

We have shown that the addition of Au NPs that selectively hydrogen bond with pyridine in PS-P2VP yields a well ordered composite. The BCP/Au NP hybrid system can be applied in organic floating gate memory devices as a charge trapping layer. This approach will enable the fabrication of well-ordered charge storage layers by solution processing and facile control of the memory windows by changing the density of Au NPs. The fabrication of large area and high density devices by using roll-to-roll printing techniques is now in progress. This extension requires the use of a solution processable dielectric such as ZrO_2 or ZrO_2/polymer hybrid systems[37,38] and patterning of the top and bottom electrodes to individually address storage clusters.

EXPERIMENTAL SECTION

Materials. Poly(styrene-*b*-2-vinyl pyridine) (PS8.2k-*b*-P2VP8.3k, Mn=16.5 kDa, PDI = 1.09) was purchased from Polymer Source. Poly(3-hexylthiophene) (P3HT) was purchased from Merck Chemicals. Tetrahydrofuran (THF) and chlorobenzene was purchased from Aldrich.

Nanoparticle Synthesis. Au−OH nanoparticles were synthesized by a single-phase reduction reaction, according to the Brust-Schiffrin method.[32] Typically, hydrogen tetrachloroaurate trihydrate (234 mg, 0.59 mmol) and *p*-mercaptophenol (282 mg, 1.8 mmol) were dissolved in methanol (150 mL). Acetic acid (10 mL) was added to the mixture to prevent the deprotonation of *p*-mercaptophenol, and 30 mL of freshly prepared 0.4 M aqueous sodium borohydride was added carefully in one portion with vigorous stirring. The solution turned brown immediately indicating the formation of gold clusters in the size range around 2 nm. After further stirring for 30 min the solvent was removed under reduced pressure, and the dark-brown residue was washed thoroughly with diethyl ether to remove excess *p*-mercaptophenol and washed with water to remove borates and acetates. The product was dried under a stream of N_2, followed by a final drying on a vacuum line. There was 132 mg of the pure product as a dark-brown solid obtained.

Sample Preparation for Small-Angle X-ray Scattering and TEM. Appropriate amounts of block copolymer and dried nanoparticle powder were weighed and dissolved in DMF to form 10% (wt/v) stock solutions. The solution was stirred for one day, then cast on a glass slide and dried at room temperature, allowing the solvent to slowly evaporate over 24 h. The blend was then annealed at 120 °C under vacuum for 24 h and slowly cooled to room temperature.

Small-Angle X-ray Scattering. The as-prepared samples were placed in the center of 2 mm thick metal washers and sealed on both sides with Kapton film. Small-angle X-ray scattering (SAXS) was performed at room temperature using an Rigaku-Molecular Metrology SAXS instrument using 0.1542 nm (Cu Kα radiation) and an incident beam of 0.4 mm diameter. The sample-to-detector distance was calibrated using the silver behenate standard peak at 1.076 nm^{-1}. Scattered X-rays were collected onto a 2-D wire array detector located at a distance of 1.195 m that corresponds to the measured *q*-range, 0.06 $nm^{-1} < q < 1.6$ nm^{-1} in which $q = (4\pi/\lambda) \sin\theta$, where 2θ is the scattering angle. The raw scattering data were circularly averaged and plotted as intensity vs *q* where intensity was used in arbitrary units. For data presentation, the profiles are shifted vertically by multiplying intensity S3 values with constant factors to avoid overlap of the profiles.

TEM. The as-prepared PS-P2VP composites were embedded in epoxy and cured at room temperature overnight. Thin sections for microscopy were prepared using a Leica Ultracut UCT microtome equipped with a Leica EM FCS cryogenic sample chamber. Bright field TEM measurements were conducted with either a JEOL 2000FX TEM or JEOL 100CX TEM operated at accelerating voltages of 100 kV and 200 kV, respectively.

Device Fabrication and Characterization. Transistors were built on highly doped n-type (100) Si substrates (<0.02 Ω cm) with 300-nm thermally grown silicon dioxide. The SiO_2 surface was covered with PS-P2VP/Au NPs, which was spin-coated from a 5 mg/mL THF solution and baked at 150 °C on a hot plate for 15 min in a nitrogen-filled glovebox. The capacitance of the gate dielectric was $C_i = 10.7 \pm 0.7$ nF cm^{-2}. The substrates with the structure of glass/PSS/P3HT were prepared by successive spin-coating of an aqueous solution of poly(styrene sulfonate) sodium salt (10 mg/mL) and a chlorobenzene solution of P3HT (2 mg/mL). Then, the polymer films were transferred onto the dielectric substrates. Gold electrodes were evaporated onto the surface through a metal mask. The electrical characteristics of the transistors were measured using a Keithley 4200 semiconductor parameter analyzer under vacuum.

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Supporting Information Available: Additional information about lower magnification TEM images; photographic images of the mixture THF solution of Au NPs and THF solution of P2VP; optical microscope images of a blend film with 60% Au NPs; double-sweeping semilog plots of I_D-V_G; transfer characteristics of the devices with different concentration of Au NPs; data retention capability measurement and calculation details about the interparticle distance. This material is available free of charge *via* the Internet at http://pubs.acs.org.

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